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PRACTICE LIMITED TO PATENTS, TRADEMARKS,
AND
U.S. AND FOREIGN INTELLECTUAL PROPERTY MATTERS

August 4, 2004

Via Express Mail: ED 043483314 US
Mail Stop Petitions
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Re: Petition for Filing Date and Response to Formalities Letter:
High Output Impedance Biasing for Magnetoresistive Elements
Attorney Docket: TI-35328

Dear Sir:

Enclosed for filing please find the following items relating to the above-identified patent application:

(1) Copy of Formalities Letter dated 06/21/04
(2) Petition;
(3) Copy of Postcard date-stamped 08/26/03;
(4) Copy of Specification;
(5) Copy of 2 Sheets of Formal Drawings;
(6) Fee Authorization/Transmittal Form;
(7) Declaration and Power of Attorney; and
(8) Postcards (2).

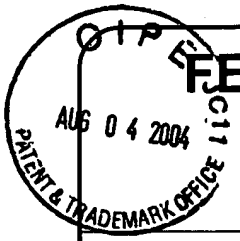
Please charge **Deposit Account No. 20-0668** in the amount of the total fees set forth. The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to **Deposit Account No. 20-0668.**

Michael T. Konczal
Registration No. 45,475

c: Cindy Dees, Texas Instruments Incorporated

EXPRESS MAIL Mailing Label No. ED 043483314 US
DATE: 08/04/04

PTO/SB/17(11-00)
Approved for use through 10/31/2002. OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.



FEE TRANSMITTAL for FY 2004

Complete If Known	
Application Number	10/647,943
Filing Date	08/26/03
First Named Inventor	Motomu Hashizume
Examiner Name	
Group Art Unit	
Attorney Docket No.	TI-35328

TOTAL AMOUNT OF PAYMENT	$ 130

METHOD OF PAYMENT

1. ☒ The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:

Deposit Account Number: 20-0668

Deposit Account Name: Texas Instruments Incorporated

☐ Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

☐ Applicant claims small entity status. See 37 CFR 1.27

2. ☐ **Payment Enclosed:**

☐ Check ☐ Credit card ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	750	201	370	Utility filing fee	$750
106	330	206	165	Design filing fee	
107	510	207	255	Plant filing fee	
108	740	208	370	Reissue filing fee	
114	160	214	80	Provisional filing fee	
				SUBTOTAL (1)	($)

2. EXTRA CLAIM FEES

	Extra Claims		Fee from below			=	Fee Paid
Total Claims	17	-20**=	0	X	18	=	0
Independent Claims	3	-3** =	0	X	84	=	0
Multiple Dependent					0	=	0

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	84	202	42	Independent claims in excess of 3
104	280	204	140	Multiple dependent claim, if not paid
109	84	209	42	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) $ 0

**or number previously paid, if greater; For Reissue, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee of oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for *ex parte* reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension for reply within second month	
117	920	217	460	Extension for reply within third month	
118	1,440	218	720	Extension for reply within fourth month	
128	1960	228	980	Extension for reply within fifth month	
119	320	219	160	Notice of Appeal	
120	320	220	160	Filing a brief in support of an appeal	
121	280	221	140	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,280	241	640	Petition to revive - unintentional	
142	1,280	242	640	Utility issue fee (or reissue)	
143	460	243	230	Design issue fee	
144	620	244	310	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	$130
123	50	123	50	Petitions related to provisional applications	
126	180	126	180	Submission of information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	740	246	370	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	740	249	370	For each additional invention to be examined (37 CFR § 1.129(b))	
179	740	279	370	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	
Other fee (specify)					

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($)130

SUBMITTED BY				Complete (if applicable)	
Name (Print/Type)	Michael T. Konczal	Registration No. (Attorney/Agent)	45,475	Telephone	214-228-3641
Signature	Michael T. Konczal			Date	08/04/04

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231

08-05-04 IFW DAC

10/647,943

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Applicant:	Motomu Hashizume	Docket No.:	TI-35328
Serial No:	10/647,943	Art Unit:	
Filed:	August 26, 2003	Examiner:	
Title:	High Output Impedance Biasing for Magnetoresistive Elements		

PETITION FOR FILING DATE AND RESPONSE TO FORMALITIES LETTER

August 4, 2004

Commissioner for Patents
Mail Stop Petitions
P.O. Box 1450
Alexandria, VA 22313-1450

Office of Petitions:

This is a response to the Formalities Letter dated June 21, 2004 (copy attached), due for reply by August 21, 2004.

In view of the following evidence and assertions, **Applicant hereby petitions for the Application to be accorded the filing date of August 26, 2003.**

The commissioner is hereby authorized to charge Deposit Account No. 20-0668 for a petition fee under 37 CFR 1.17(h) and any additional fees required in this matter. In the event that the present Petition is granted, Applicant respectfully requests a refund of the petition fee.

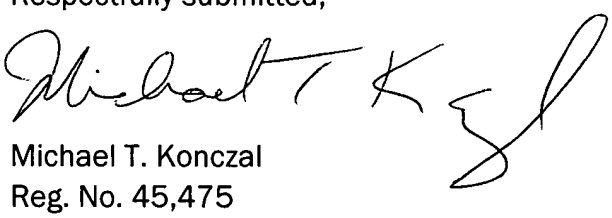
08/06/2004 HALI11 00000009 200668 10647943
01 FC:1460 130.00 DA

Applicant asserts the informed belief that Formal Drawings were filed via express mail on August 26, 2003. Attached is a true and correct copy of the Return Postcard date-stamped 08/26/03 by the USPTO indicating the receipt of Formal Drawings in this matter. Also attached are true and correct copies of the Drawings believed to have been submitted on August 26, 2003.

Additionally, Applicant asserts that drawings are not necessary to the understanding of the invention under the meaning of 35 USC 113. Applicant respectfully cites MPEP 601.01(f), explicitly indicating the USPTO practice to treat an application that contains at least one method claim as an application for which a drawing is not necessary under 35 USC 113. Attached is a true and correct copy of the Specification and Claims submitted on August 26, 2003, which includes at least one method claim.

Alternatively, should the present Petition be found wanting, Applicant respectfully requests that the attachments submitted herewith, which include a Specification, Drawings, and newly executed Declaration, be duly forwarded to Mail Stop Missing Parts and accorded a filing date of their receipt by express mail.

Respectfully submitted,



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UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/647,943	08/26/2003	Motomu Hashizume	TI-35328

CONFIRMATION NO. 3032

23494
TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

FORMALITIES LETTER

OC000000012988269

Date Mailed: 06/21/2004

NOTICE OF INCOMPLETE NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

A filing date has NOT been accorded to the above-identified application papers for the reason(s) indicated below.

All of the items noted below **and a newly executed oath or declaration covering the items must** be submitted within **TWO MONTHS** of the date of this Notice, unless otherwise indicated, or proceedings on the application will be terminated *(37 CFR 1.53(e))*. Replies should be mailed to: Mail Stop Missing Parts, Commissioner for Patents, P.O. Box 1450, Alexandria VA 22313-1450.

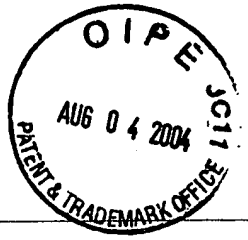
The filing date will be the date of receipt of all items required below, unless otherwise indicated. Any assertions that the item(s) required below were submitted, or are not necessary for a filing date, must be by way of petition directed to the attention of the Office of Petitions accompanied by the $130.00 petition fee *(37 CFR 1.17(h))*. If the petition states that the application is entitled to a filing date, a request for a refund of the petition fee may be included in the petition. Petitions should be mailed to: Mail Stop Petitions, Commissioner for Patents, P.O. Box 1450, Alexandria VA 22313-1450.

- The application was deposited without drawings. 35 U.S.C. 113 (first sentence) requires a drawing "where necessary for the understanding of the subject matter sought to be patented." *Applicant should reconsider whether the drawings are necessary under 35 U.S.C. 113 (first sentence).*

Replies should be mailed to: Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

A copy of this notice MUST be returned with the reply.

Customer Service Center
Initial Patent Examination Division (703) 308-1202



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X NEW APPLICATION	___ AMENDMENT ___
X DECLARATION	___ EOT ___
X ASSIGNMENT	___ NOTICE OF APPEAL
X FORMAL DRAWINGS	___ APPEAL ___
___ INFORMAL DRAWINGS	___ ISSUE FEE
___ CONTINUATION APP'N	___ REPLY BRIEF (IN TRIPLICATE)
___ DIVISIONAL APP'N	___

ME OF INVENTOR(S):
otomu Hashizume; Naoko Jinguji

RECEIPT DATE & SERIAL NO.:
Serial No.:

LE OF INVENTION:
igh Output Impedance Biasing for agnetoresistive Elements

FILE NO.:	DEPOSIT ACCT. NO.:
I-35328	**20-0668**

XPRESS MAIL RECEIPT NO.:
U019804415US
LD:
UE:
TTY/SEC'Y: Mike Konczal

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___ INFORMAL DRAWINGS	___ ISSUE FEE
___ CONTINUATION APP'N	___ REPLY BRIEF (IN TRIPLICATE)
___ DIVISIONAL APP'N	___

NAME OF INVENTOR(S):
Motomu Hashizume; Naoko Jinguji

RECEIPT DATE & SERIAL NO.:
Serial No.:

TITLE OF INVENTION:
High Output Impedance Biasing for Magnetoresistive Elements

TI FILE NO.:	DEPOSIT ACCT. NO.:
TI-35328	**20-0668**

EXPRESS MAIL RECEIPT NO.:
EU019804415US
MLD:
DUE:
ATTY/SEC'Y: Mike Konczal

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10/647943
08/26/03

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X NEW APPLICATION	
X DECLARATION	
X ASSIGNMENT	
X FORMAL DRAWINGS	
___ INFORMAL DRAWINGS	
___ CONTINUATION APP'N	
___ DIVISIONAL APP'N	

AME OF INVENTOR(S):
Motomu Hashizume; Naoko Ji

ITLE OF INVENTION:
ligh Output Impedance Biasin Magnetoresistive Elements

TI FILE NO.:	DEPOSIT ACCT. NO.:
TI-35328	**20-0668**

EXPRESS MAIL RECEIPT NO.:
EU019804415US
MLD:
DUE:
ATTY/SEC'Y: Mike Konczal

HIGH OUTPUT IMPEDANCE BIASING FOR MAGNETORESISTIVE ELEMENTS

TECHNICAL FIELD

[001] The invention relates to electronic circuit biasing. More particularly, the invention relates to methods and circuits for magnetoresistive (MR) element biasing.

BACKGROUND OF THE INVENTION

[002] For the purposes of describing this invention, the term "magnetoresistive element" encompasses any electronic element used for detecting variations in a magnetic field by detecting a change in the resistance of the element caused by variations in the magnetic field. Also for the purposes of this disclosure, the term "MR head" is used interchangeably with "magnetoresistive element". Examples of MR elements that are contemplated to be within the scope of this invention include, but are not limited to, dual MRs, giant MRs (GMR), tunnel junction giant MRs (TGMR), current perpendicular to plane mode (CPP) MRs and any read head which requires biasing to read out signals.

[003] MR elements have been found to be particularly useful for reading binary data stored on magnetic media. The resistance of MR elements is dependent upon the direction and magnitude of an applied magnetic field. As the MR element is moved relative to an adjacent magnetic medium, or *vice-versa*, the resistance of the MR element changes. Thus, the MR element may be coupled to additional circuitry to decode the changes in resistance in order to retrieve stored data. The resistance changes in MR elements are generally nonlinear in

character. It is common, therefor, to electrically bias the MR element for operation within a preferred range of its capability. In biasing, a current or voltage is applied to the MR element to set a baseline of resistance. Changes in resistance induced by the adjacent magnetic medium may then be compared against this baseline.

[004] Various biasing schemes exist in the arts. Constant-current biasing entails coupling an MR element between two balanced current sources. One terminal of an MR head is coupled to a current source and the other terminal is coupled to a current sink. Constant-voltage biasing is applicable using current sources with a voltage feed back loop. Constant-current or constant-voltage biasing in circuits using low output impedance current sources has the advantage of making the MR head potential easy to control. Such biasing schemes suffer from attenuating the data signal output from the MR head, making the signal more susceptible to the effects of noise degradation. However, although constant-current or constant-voltage biasing in circuits using high output impedance current sources reduces susceptibility to noise, it introduces problems in controlling the MR head potential. When there is a sufficient voltage difference between the MR head and the magnetic medium, arcing can occur causing loss of data or damage to the head or medium.

[005] Due to these and other challenges in biasing MR elements, it would be useful and desirable in the arts to provide biasing methods and circuits resistant to signal loss and noise degradation while maintaining MR head voltage at a predetermined level. It would be particularly advantageous for such methods and circuits to provide capabilities for accommodating changes in biasing levels,

fast recovery times, and decreased power consumption.

SUMMARY OF THE INVENTION

[006] In carrying out the principles of the present invention, in accordance with preferred embodiments thereof, methods and circuits are provided for biasing MR elements responsive to feedback indicating actual bias conditions.

[007] According to one aspect of the invention, an MR element biasing circuit and method uses an MR element and a constant-voltage biasing loop as known in the arts combined with a common-mode feedback loop. The common-mode feedback loop is operatively coupled to the MR element and the constant-voltage biasing loop in such a way as to maintain the potential of the MR element at approximately zero Volts.

[008] According to another aspect of the invention, an MR element biasing circuit and method uses a common-mode feedback loop operatively coupled to an MR head and a constant-voltage biasing loop. The circuit includes bipolar transistors interconnected in a configuration for maintaining the MR head potential at approximately zero Volts.

[009] According to yet another aspect of the invention, a method for biasing an MR head includes the step of providing constant-voltage biasing to an MR head subcircuit. In a further step, the current is mirrored in a common-mode feedback subcircuit and any current differential is substantially eliminated, thereby limiting the potential difference at the MR head to approximately zero Volts.

[010] According to still another aspect of the invention, methods of MR head biasing also include a step of providing a reference current in a common-mode feedback subcircuit.

[011] Preferred embodiments of the invention are described in which bipolar transistors are used in circuits and in performing method steps. Preferred embodiments of the invention may be implemented using either MOSFETs or JFETs.

[012] The invention provides technical advantages including but not limited to providing high output impedance leading to good noise performance, offering stable regulation of head potential, and avoiding excessive power consumption. These and other features, advantages, and benefits of the present invention will become apparent to one of ordinary skill in the art upon careful consideration of the detailed description of representative embodiments of the invention in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[013] The present invention will be more clearly understood from consideration of the following detailed description and drawings in which:

[014] Figure 1 is an example of an MR element biasing circuit and method according to a preferred embodiment of the invention; and

[015] Figure 2 is an example of an MR element biasing circuit and method

according to a preferred alternative embodiment of the invention; and

[016] Figure 3 is a process flow diagram illustrating an example of steps in a preferred method of the invention.

[017] References in the detailed description correspond to like references in the figures unless otherwise noted. Like numerals refer to like parts throughout the various figures. Descriptive and directional terms used in the written description such as upper, lower, left, right, etc., refer to the drawings themselves as laid out on the paper and not to physical limitations of the invention unless specifically noted. The drawings are not to scale, and some features of embodiments shown and discussed are simplified or exaggerated for illustrating the principles, features, and advantages of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[018] In general, the invention uses a high output impedance circuit for MR head biasing, providing low susceptibility to noise. The invention also provides the advantages of fast recovery times when the MR head undergoes a voltage change or is switched between an "on" state and an "off" state. The methods and circuits of the invention also use less power than other solutions known in the arts, and provide MR heads common-mode voltage stability.

[019] Referring first primarily to Figure 1, an example of an MR head biasing circuit 10 is illustrated. A current source MR head circuit 12 is shown. The MR head subcircuit 12 shown is provided by way of example only and it should be

understood that alternative MR head circuit arrangements 12 may be used without departure from the scope of the invention. An MR head 14 is included in the MR head subcircuit 12 and is configured for operation as is known in the arts. Multiple MR heads may be used for read/write operations. A constant-voltage biasing loop 16 is also provided as is known in the arts. Of course, the exact configuration of the constant-voltage biasing loop 16 is not essential to the practice of the invention. A common-mode feedback loop 18 joins the constant-voltage biasing subcircuit and the MR head subcircuit 12, 16. The common-mode feedback loop 18 is adapted to maintain voltage potential of the MR head 14 at approximately zero Volts relative to the common voltage of the circuit 10. The voltage feedback, or common-mode feedback loop, is realized using opposite polarity components, e.g., NPN to PNP. Thus the polarity of the transistors shown and described may be reversed without departing form the invention. Preferably, all of the transistors shown may have an emitter degeneration resistor to improve current tolerance.

[020] Further examination of Figure 1 will reveal that bipolar transistors Q1, Q2, Q3, Q4 are arranged as gm (voltage-current converter) amp. The current mirror of Q1 and Q2 is coupled to the top rail 24, and the differential pair of Q3 and Q4 is coupled to bottom tail 26, via a current source 28, of the circuit 10. This configuration converts voltage difference between Q3-base and Q4-base to sink or source current. Thus, a stabilizing network 30 coupled between the differential pair and the MR head, and current source Q22 driven by gm output is capable of maintaining the potential at a point, herein referred to for convenience as the central node 32, at or very near zero. Various alternative embodiments of the stabilizing network 30 may be used so long as the requirement of maintaining

the central node 32 voltage at or near zero is met. As shown in Figure 1, a preferred embodiment of the invention uses a pair of resistors 34, 36, coupled to the central node 32 and in parallel with the MR head 14.

[021] Now referring primarily to Figure 2, an alternative embodiment of a circuit 10 according to the principles of the invention is shown. As shown, the stabilizing network 30 having a resistor pair, 34, 36, about the central node 32 may be supplemented by a ground resistor 38 electrically connected between the central node 32 and circuit ground 26. The top resistor 34 is preferably connected to a bipolar transistor Q5 providing a controlled connection to the top rail 24. Similarly, the bottom resistor 36 is preferably controllably coupled to the bottom rail 26 using a bipolar transistor Q6. Preferably, Q5 and Q6 are sized and the layout is chosen to represent or scale Q22 and Q20 currents. Thus, while the central node 32 maintains approximately zero volts, MR head 14 potential is also maintained at near zero volts. This alternative embodiment of the invention reduces the potential for delay in the circuit 10 response to changes from OFF to ON in the MR head 14 biasing current. Preferably, if current sink Q20 and current source Q22, are controlled by switches, 102, 103, 104 and are turned off, the current through bipolar transistors, Q5, Q6, maintains the voltage at capacitor C1 at a predetermined level; thus recovery times will be improved in applications where this embodiment is used.

[022] An alternative view of the methods of the invention is illustrated in Figure 3. As shown in step 42, the constant-voltage biasing loop provides a bias voltage to the MR head subcircuit. The arrangement of current mirrors in the intervening common-mode feedback loop meanwhile eliminates any current

differential, shown at step 44. As indicated at step 46, this ensures that the voltage across the MR head remains at or very near zero Volts 48.

[023] Thus, the invention provides high output impedance biasing for MR elements. Figure 1 and Figure 2 show constant-voltage biasing schemes, but alternatively, omission of the head-voltage feedback loop and current control for current sink 20 (Figure 1, and Q6 in Figure 2,) function in a constant-current biasing scheme. Or in Figure 2, voltage feedback across R34 and R36, instead of the MR head 14 terminals, may be used as a constant-current biasing loop. The invention may be readily applied to MR element biasing in a variety of applications using MR head subcircuits known in the arts. While the invention has been described with reference to certain illustrative embodiments, the methods and devices described are not intended to be construed in a limiting sense. For example, various NPN or PNP transistor combinations may be substituted without departure from the methods and circuits of the invention. Various modifications and combinations of the illustrative embodiments as well as other advantages and embodiments of the invention will be apparent to persons skilled in the art upon reference to the description and claims.

WE CLAIM:

1. An MR head biasing circuit comprising:

an MR head;

a constant-voltage and constant-current biasing loop; and

a common-mode feedback loop operatively coupled to the MR head and the constant-voltage and constant-current biasing loop for maintaining the MR head potential at approximately zero Volts.

2. The MR head biasing circuit according to claim 1 wherein the common-mode feedback loop further comprises:

a first current source operatively coupled to a first terminal of the MR head; and

a second current source operatively coupled to a second terminal of the MR head and to the first current source;

whereby the first and second current sources are arranged for minimizing current differential between the first current source and the second current source ~~mirror~~.

3. The MR head biasing circuit according to claim 2 further comprising a central node defined by an operative coupling of the current sources with the first and second terminals of the MR head for maintaining the MR head potential at approximately zero Volts.

4. The MR head biasing circuit according to claim 3 further comprising a reference current source operatively coupled between the central node and a bottom rail.

5. The MR head biasing circuit according to claim 1 wherein the common-mode feedback circuit further comprises:

a first bipolar transistor having an emitter coupled to a top rail of the circuit;

a second bipolar transistor having a base coupled to a base of the first bipolar transistor, the second bipolar transistor also having an emitter coupled to the top rail and a collector coupled to the base;

a third bipolar transistor having a base coupled to a bottom rail via a resistor and a collector coupled to a collector of the first bipolar transistor;

a common-mode feedback current source having a first terminal coupled to an emitter of the third bipolar transistor and having a second terminal coupled to the bottom rail;

a fourth bipolar transistor having an emitter coupled to the first terminal of the common-mode feedback current source and to the emitter of the third bipolar transistor, and also having a collector coupled to the collector of the second bipolar transistor;

a central node defined by the operative coupling of a base of the fourth bipolar transistor, and the first and second terminals of the MR head for maintaining constant voltage.

6. The MR head biasing circuit according to claim 5 wherein the bipolar transistors comprise JFETs.

7. The MR head biasing circuit according to claim 5 wherein the bipolar transistors comprise MOSFETs.

8. The MR head biasing circuit of claim 5 further comprising a stabilizing network coupled between the central node and the first and second MR head terminals.

9. The MR head biasing circuit of claim 8 wherein the stabilizing network further comprises:

a first resistor coupled between the central node and a first terminal of the MR head and a second resistor coupled between the central node and a second terminal of the MR head.

10. The MR head biasing circuit of claim 8 wherein the stabilizing network further comprises:

a first resistor coupled between the central node and a collector of a fifth bipolar transistor;

a second resistor coupled between the central node and a collector of a sixth bipolar transistor;

a third resistor coupled between a location between the first and second resistors and ground; wherein

an emitter of the sixth bipolar transistor is coupled to a bottom rail;

a base of the sixth bipolar transistor is operatively coupled to the constant-voltage biasing loop and also to the MR head;

an emitter of the fifth bipolar transistor coupled to the top rail; and

a base of the fifth bipolar transistor operatively coupled to the collector of the first bipolar transistor and also to the MR head.

11. The MR head biasing circuit according to claim 10 wherein the bipolar transistors comprise JFETs.

12. The MR head biasing circuit according to claim 10 wherein the bipolar transistors comprise MOSFETs.

13. An MR head biasing circuit comprising:

an MR head;

a constant-voltage and constant-current biasing loop; and

a common-mode feedback loop operatively coupled to the MR head and the constant-voltage and constant-current biasing loop for maintaining the MR head potential at approximately zero Volts, the common-mode feedback loop further comprising:

a first bipolar transistor having an emitter coupled to a top rail of the circuit;

a second bipolar transistor having a base coupled to a base of the first bipolar transistor, the second bipolar transistor also having an emitter coupled to the top rail and a collector coupled to the base;

a third bipolar transistor having a base coupled to a bottom rail via a resistor and a collector coupled to a collector of the first bipolar transistor;

a common-mode feedback current source having a first terminal coupled to an emitter of the third bipolar transistor and having a second terminal coupled to the bottom rail;

a fourth bipolar transistor having an emitter coupled to the first terminal of the common-mode feedback current source and to the emitter of the third bipolar transistor, and also having a collector coupled to the collector of the second bipolar transistor;

a central node defined by the operative coupling of a base of the fourth bipolar transistor, and the first and second terminals of the MR head for maintaining constant voltage;

a first resistor coupled between the central node and a collector of

a fifth bipolar transistor;

a second resistor coupled between the central node and a collector of a sixth bipolar transistor;

a third resistor coupled between a location between the first and second resistors and ground; wherein

an emitter of the sixth bipolar transistor is coupled to the bottom rail;

a base of the sixth bipolar transistor is operatively coupled to the constant-voltage biasing loop and also to the MR head;

an emitter of the fifth bipolar transistor coupled to the top rail; and

a base of the fifth bipolar transistor operatively coupled to the collector of the first bipolar transistor and also to the MR head.

14. The MR head biasing circuit according to claim 13 wherein the bipolar transistors comprise JFETs.

15. The MR head biasing circuit according to claim 13 wherein the bipolar transistors comprise MOSFETs.

16. An MR head biasing method comprising the steps of:

providing constant-voltage biasing to an MR head subcircuit;

mirroring the current in a common-mode feedback subcircuit and substantially eliminating any current differential;

thereby maintaining the potential difference at the MR head to approximately zero Volts.

17. An MR head biasing method according to claim 16 further comprising the step of providing reference current in the common-mode feedback subcircuit.

HIGH OUTPUT IMPEDANCE BIASING FOR MAGNETORESITIVE ELEMENTS

ABSTRACT

[024] Disclosed are methods and circuits (10) for biasing magnetoresistive elements (14). The methods and circuits (10) of the invention provide high output impedance current sources using an MR element (14) and a constant-voltage biasing loop (16) combined with a common-mode feedback loop (18). The common-mode feedback loop (18) is configured to maintain the potential of the MR element (14) at approximately zero Volts. Disclosed embodiments of the invention use complementary current mirrors (Q20, Q22) to substantially eliminate current differentials in the common-mode feedback loop (18) in order to hold the MR head potential at approximately zero Volts. Also disclosed are methods and circuits (10) in which a reference current source (28) is provided in a common-mode feedback subcircuit (18). Preferred embodiments of the invention are described in which bipolar transistors (Q), for example MOSFETs or JFETs, are used in circuits for performing method steps.

FIG. 1

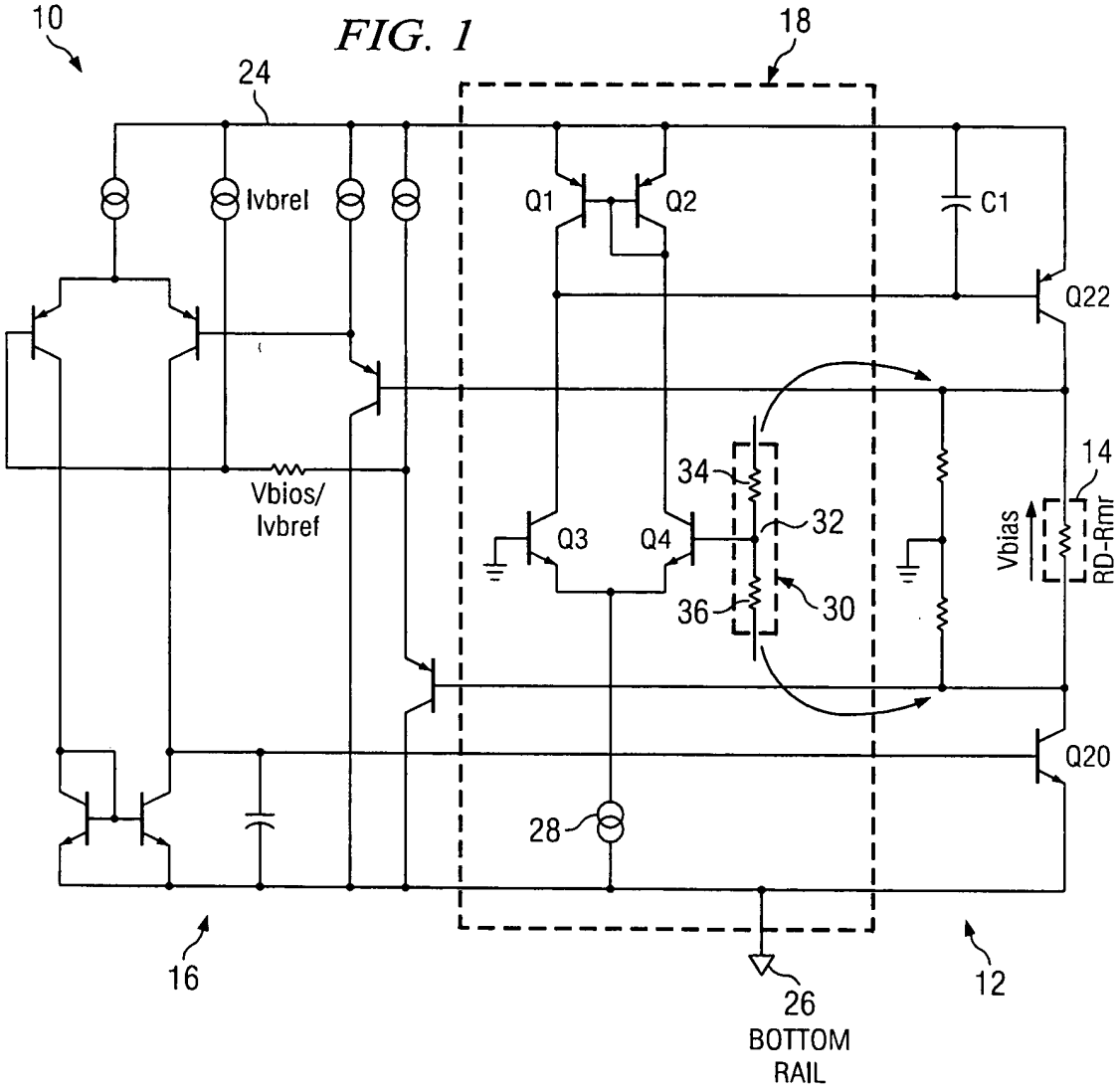


FIG. 2

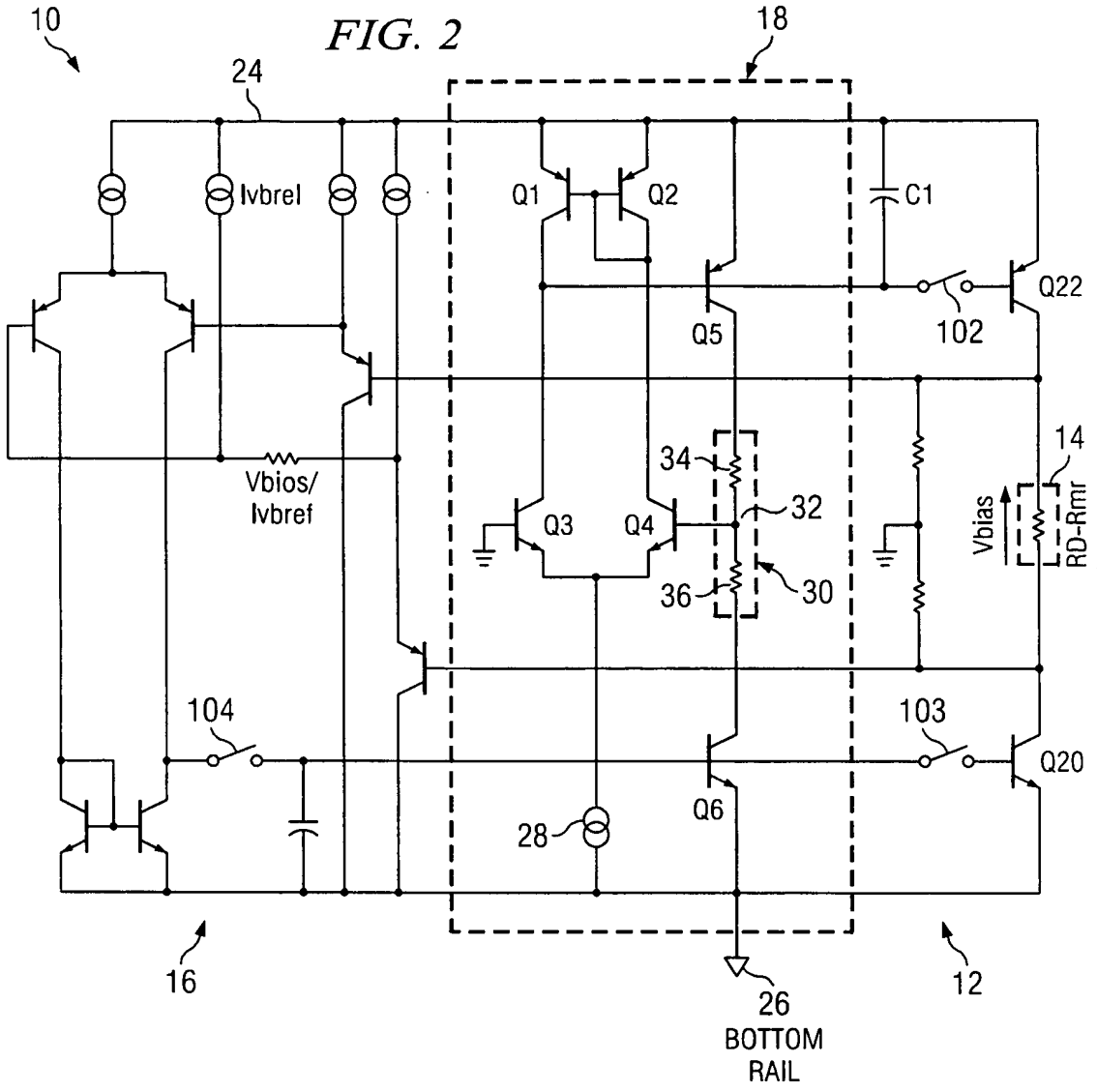


FIG. 3

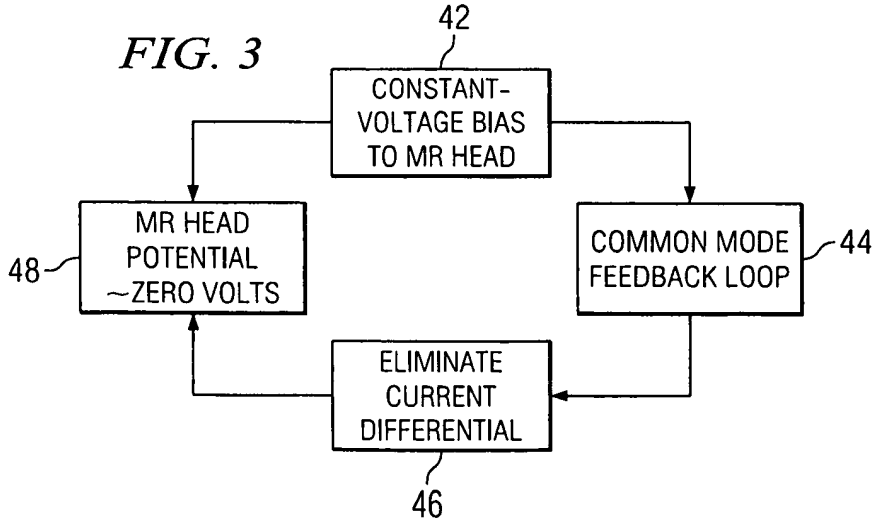


FIG. 1

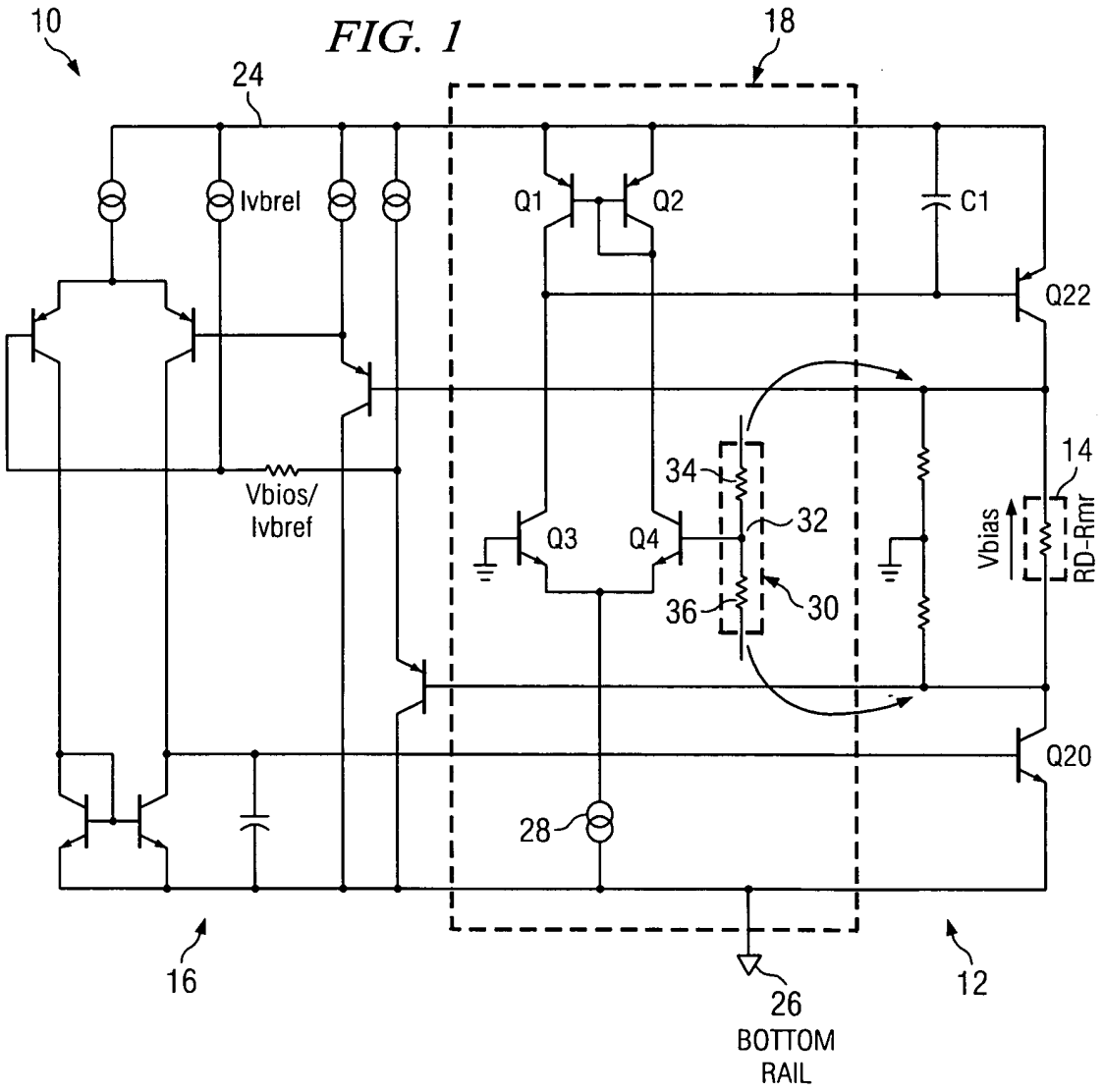


FIG. 2

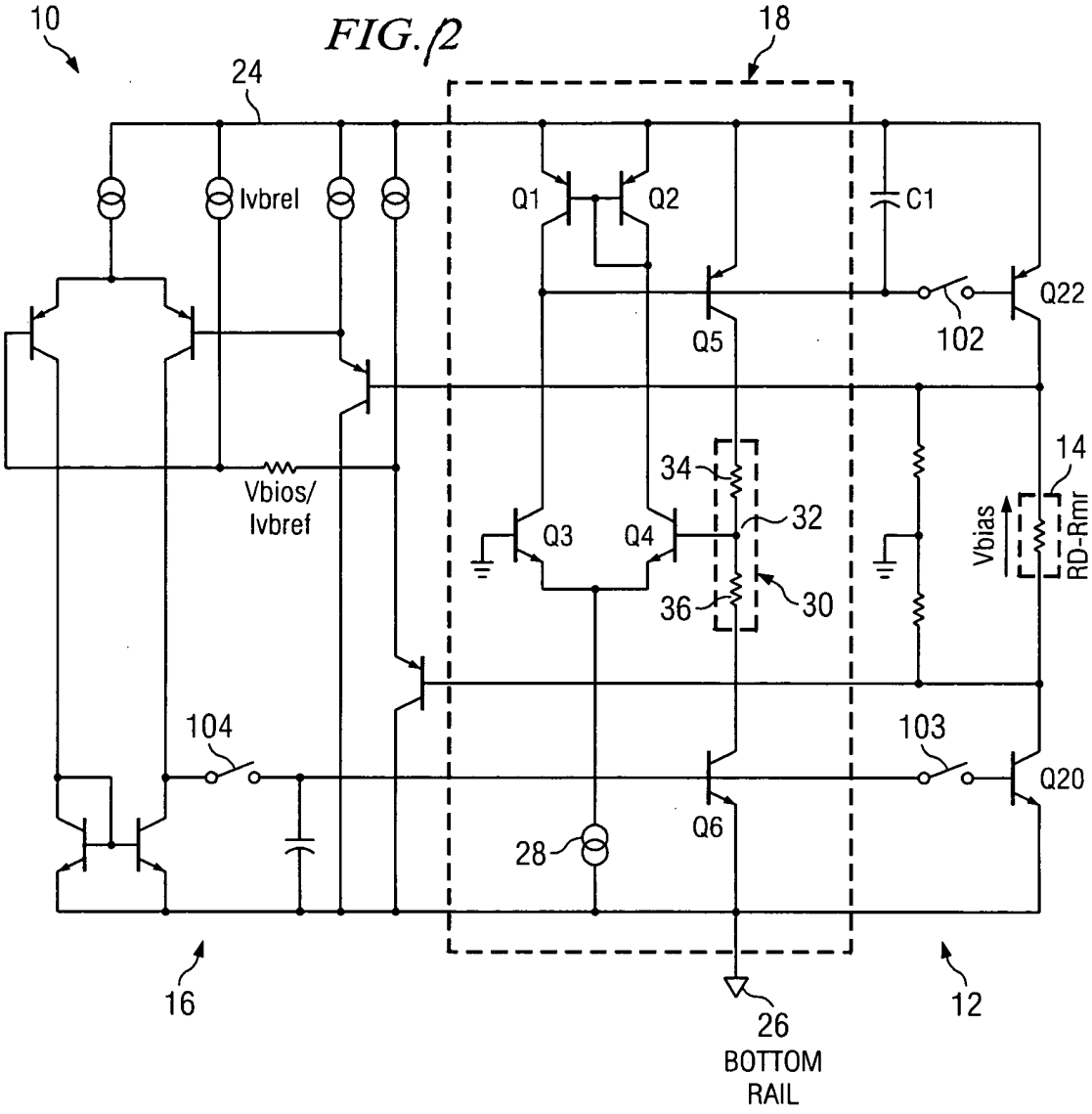
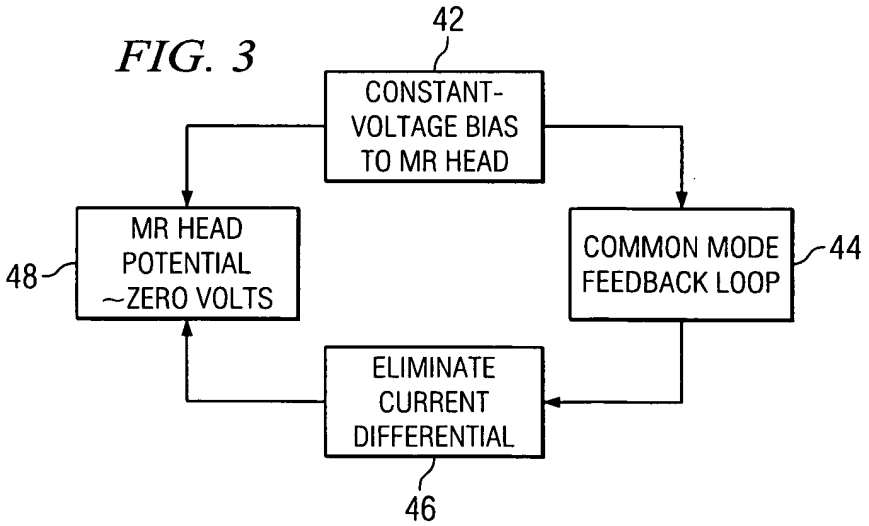


FIG. 3



ATTORNEY'S DOCKET NO.
TI-35328

APPLICATION FOR UNITED STATES PATENT
DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor if only one name is listed below, or an original, first and joint inventor if plural inventors are named below, of the subject matter which is claimed and for which a patent is sought on the invention entitled as set forth below, which is described in the attached specification; that I have reviewed and understand the contents of the specification, including the claims, as amended by any amendment specifically referred to in the oath or declaration; that no application for patent or inventor's certificate on this invention has been filed by me or my legal representatives or assigns in any country foreign to the United States of America; and that I acknowledge my duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

TITLE OF INVENTION: High Output Impedance Biasing for Magnetoresistive Elements

POWER OF ATTORNEY: I HEREBY APPOINT THE FOLLOWING ATTORNEYS TO PROSECUTE THIS APPLICATION AND TRANSACT ALL BUSINESS IN THE PATENT AND TRADEMARK OFFICE CONNECTED THEREWITH

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DATE: 7/16/04	DATE: 7/16/04	